CADY

Introducing Automatic Electrical Schematic Inspection

Introduction

The electronic industry faces an increasing demand for an efficient and effective product development process to introduce new products to the market. To stay competitive, these products must be innovative, feature-rich, reliable, and cost-effective. However, the current development process has its challenges. From the outset, once the new product's functionality has been determined, electronic schematic designers (also known as Hardware developers/designers) face a lack of automated tools for verifying the integrity of their schematic designs. Consequently, they must manually inspect each component meticulously to ensure it aligns with the instructions provided in the components manufacturers' datasheets. Moreover, ensuring compliance with specific industry requirements, especially in sectors like Aerospace or Automotive, poses even greater challenges. Additionally, confirming that the components can be procured within an acceptable time frame and are not reaching their end-of-line stage adds further complexity to the process. The Problem

Electric circuits serve as the foundation for every modern electrical device. In recent decades, as the physical size of electrical components decreased (exemplified by "Moore's law") and functional demands have risen significantly, the complexity of circuit designs has drastically increased. This arises from the need to accommodate a higher number of components constrained by limited real estate. These components encompass simple passive elements like resistors, capacitors, inductors, diodes, as well as sophisticated active components like microprocessors, FPGAs, voltage regulators, sensors, and more.

When developing a new electronic product, the typical process involves designing the electrical schematic using an ECAD (Electronic Computer-Aided Design) system, followed by a schematic design review upon completion. The design then moves on for layout roughing,



leading to the manufacturing and assembly of a printed circuit board (PCB) for the initial "Bring-Up." During this phase, the envisioned electronic circuit is physically realized and tested using laboratory equipment and other physical testing methods. However, the combination of increased functionality demands, and limited real estate has made schematic designs highly complex and extremely challenging to create and debug within a reasonable timeframe. Consequently, achieving an error-free design on the first iteration has become nearly impossible.

Currently, a significant portion of the schematic design review relies on designers manually reading electric components' datasheets to verify that each component meets the required specifications, and that the design's functionality aligns with the desired requirements. Unfortunately, errors often go unnoticed, ranging from simple wrong connections to complex logical errors, preventing the circuit from performing as intended. When errors are detected, the schematic and layout must be corrected accordingly, resulting in a "re-spin" of the design. These re-spins are costly, time-consuming, and wasteful, and they frequently delay the product's market launch.

In some cases, design errors may remain hidden until the product is already on the market. This can result in product recalls, on-site repairs, damage to the company's reputation, and substantial financial expenses. Evidently, a need exists for an automated system that can detect errors during the early stages of the process. Such a system would help decrease the number of project re-spins and greatly reduce the risk of defective products reaching the market.

The Solution

Existing Electrical Schematics Review Tools

Several techniques are available for reviewing and validating PCB designs, encompassing functional analysis, timing simulations, and logical equivalence checking, where the new circuit model is compared to a reference model representing the desired functionality. Although these techniques prove valuable, they may not sufficiently identify errors or suboptimal designs related to datasheet information, such as missing pull-up/down resistors, communication protocol line mismatches, exceeding operating conditions (voltage, current, temperature, etc.), violating direct connection instructions, incorrect component placements, and traces routing issues, among others. While verification software tools like "Design Rules Check" (DRC), such as "Valydate Schematic Analysis" in Mentor Graphics' Xpedition package, can partially detect some of these errors, they have limited capabilities in detecting design errors across a broader spectrum. They lack the



ability to access, process, understand, and implement datasheet information effectively. Consequently, the electronic industry still heavily relies on manual design reviews, a slow, cumbersome, and error-prone process, leading to repetitive design iterations or "re-spins."

As a result, the electronic industry is in dire need of an automatic electrical circuit design inspection system. This system should possess the ability to detect a wide range of errors, incorporate best-practice guidelines, and provide simultaneous bottom-up and top-down perspectives. It should be capable of verifying specific component requirements while aligning them with the overall design requirements.

CADY's System Methodology

CADY developed a solution that effectively addresses the industry's needs and resolves the problem at hand. The system's functionality revolves around scanning electrical component datasheets and extracting pertinent information related to the schematic design. Below is a summary of the process: The process commences by scanning the datasheets and analyzing the information relevant to the schematic design. It then extracts the desired information item (for example, a pin's voltage range). The extracted information is further processed using specialized NLP (Natural Language Processing) and image processing algorithms to infer the requirement or property it represents.

A comprehensive component database is created by the system, where each component is recorded with all requirements and definitions translated into a formal language. For instance, the database would specify that pin 1 is named VCC, necessitating a power supply of 1.5V to 6.5V and must be connected to the ground via a 4.7uF capacitor.

Upon uploading a design to the system, the system cross-checks it with the components' required implementation (properties and requirements) as detailed in the database. The entire schematic's nets and pins are automatically traversed and analyzed for each component and connection. Remarkably, even for complex designs with over 20K pads, the analysis process takes just a few minutes. If the system detects any discrepancies between the component's record and the actual schematic, it generates a comprehensive "suspected issues" report. This report provides detailed information about each identified issue, including the specific net, component, and pin where it occurred. Users can effortlessly download the report, review it, and, if necessary, rectify the errors.

CADY's system is entirely automatic, eliminating the need for any manual data insertion. It only requires the upload of Netlist and BOM (Bill of Materials) project files to function



efficiently and effectively., timing simulations, and logical equivalence checking, which compares the new circuit model to a reference model representing the desired functionality Despite the usefulness of these methods, they may not identify certain errors or non-optimal designs that are related to information from datasheets. Such errors include missing pull-up/down resistors, communication protocol line mismatches, violations of operating conditions (e.g., voltage, current, temperature), incorrect



component placements, and traces routing issues, among others. While some of these errors may be partially detected by "Design Rules Check" (DRC) tools integrated into most PCB design ECAD (Electronic Computer-Aided Design) software, their detection range is limited, and they lack the ability to access, process, and comprehend datasheet information effectively. The electronic industry still heavily relies on manual design reviews, which is a slow, cumbersome, and an error-prone process, leading to repetitive design reiterations or "re-spins."

Competitive Advantages

This groundbreaking system represents the first-ever achievement of automatic reading and comprehension of components' datasheets. Its advantages are abundant, and a few key ones include:

Enhanced Error Detection. The system surpasses the limitations of manual review by comprehensively addressing and analyzing a broader range of information. This capability introduces an additional layer of safety during the schematic design review process. It enables the identification of a diverse set of requirements, thereby significantly reducing the occurrence of faulty schematic designs and eliminating the need for repetitive design reiterations or "re-spins."



Scalability. The system's design allows for scalability on multiple fronts. Firstly, it enables the incorporation of new types of data to be examined, expanding its capabilities to adapt to evolving needs. Secondly, it offers support for new electrical components by automatically extracting and converting their electrical documentation. Lastly, the system ensures a consistent update of data for existing components, ensuring ongoing relevance and accuracy.

						INSPECTION REPORT Board name: Test1 Time Stamp: Mar 06 2023, 14:55:3		
Fin	dings	1						
	Index	Part Reference	Pin Number	Nets	Components	Category	Description	Status
	1	R1	2	BL_EN	CRGCQD402F4K7	Invalid Passive Component Connection	This pin should not be left floating	
	2	U7	3	5V	POWER_SUPPLY	Invalid Supply Voltage	Supply voltage 5V is out of operating range (7.5V to 15V)	···· · · · ·
	3	C41	2	5V	GRM155R60J475ME47D	Potential Capacitor Breach	Voltage difference of 5V is too close to the rated voltage 6.3V 50% derating factor is recommended	
+	4-7					Communication Protocol	I2C lines mismatch	v)
*	8-10	U7			POWER_SUPPLY	Connection Instruction Violation	This pin should be connected directly to Ground	
	11	U8	6	I2C_SCL	HDC1080DMBT	Missing Pull Resistor	Pull-up resistor is missing	
	12	U9	37	N16931850	SIM7000E	Missing Pull Resistor	Pull-up resistor is missing	
÷	13-14			DGND		Power Pin Connection	This pin should not be connected directly to Ground	
	15			VLED-		Redundant Pull Resistors	2 pull-down resistors (R5, R62) Found on net	
+	16-20				BSS138	Transistor violation	Drain pin not driven	*
	21	U4	28	GND_POWER	MCP39F501-E/MQ	Connection Instruction Violation	This pin should be left floating	
	22	U1	5	GND	TPS61165DBV	Connection Instruction Violation	This pin should be connected to Ground via a Capacitor	
÷	23-26					Inadequate Temperature Range		Y
+	27-28	U9			SIM7000E	Best Practice	Reset pins should be connected to Ground via a Capacitor	
+	29-42					Best Practice	Missing Test Point	···· · · ·

Empirical Results

The CADY system has already proven to be immensely valuable to its users. In over 65% of the electrical schematics inspected by the system so far, it successfully detected at least one significant error, leading to immediate design corrections. Without CADY, these errors would likely have surfaced during the "Bring-Up" phase, resulting in costly design reiterations, or worse, after the product's release, leading to recalls or on-site repairs. Moreover, 87% of the users have conducted follow-on inspections with additional designs.

The current technology marks only the initial stages of a significantly broader potential While the current product has already delivered unparalleled value, the system's ability to read and "understand" electrical component datasheets opens the door to future expansions. The team plans to leverage this capability to perform layout design inspections, in addition to developing other products related to thermal PCB design verification, mechanical PCB design verification, enhanced PCB simulations, PCB BOM optimization, and other aspects within the realm of Electronic Design Automation (EDA).